over the bottom portion of source/drain pockets 32. Either one of these well-known methods reduces the capacitance of the transistor, thereby improving transistor performance."

In the claims:

1. (Five Times Amended) A field effect transistor comprising:

a region of semiconductor material doped a first conductivity type;

[a] spaced apart source and drain regions of [said first] opposite conductivity type [and a drain of said first conductivity type], both said source region and said drain region disposed in said region of semiconductor material and a counterdoped region of [opposite] first conductivity type disposed within said source region forming a source and within said drain region forming a drain and isolated from the remaining portion of said region of semiconductor material by said source region and said drain region;

a counterdoped channel region disposed in said region of semiconductor material between said source region and said drain region;

said counterdoped channel region having a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region being the primary conduction channel of said transistor and having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source and said drain.

Amend claim 7 as follows:

7. (Four Times Amended) A semiconductor device comprising:

a substrate of a first conductivity type containing a plurality of field effect transistors, at least one of the field effect transistors having a counterdoped channel of opposite conductivity

type, a source region of said first conductivity type adjacent to the channel, a drain region of said first conductivity type adjacent to the channel and spaced from said source, all disposed in said substrate, and a gate overlying the channel;

said counterdoped channel comprising a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source region and said drain region.

Amend claim 14 as follows:

14. (Four Times Amended) A method for forming a field effect transistor, comprising the steps of:

providing a region of semiconductor material doped a first conductivity type;

forming a source region of said first conductivity type and a drain region of said first conductivity type, both said source and said drain disposed in said region of semiconductor material and separated by a counterdoped channel region disposed in said region of semiconductor material;

forming said counterdoped channel region by forming a first region in said channel region of one of undoped or opposite conductivity type;

doping said channel region with a second dopant to form a second doped region underlying the first region of said opposite conductivity type, said second doped region having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source region and said drain region.

Referring to FIGURE 1E, n-type source/drain regions 34 are formed using ion implantation. In this example, source/drain pockets 32 are implanted with an n-type material such as arsenic. Although source/drain pockets 32 are shown extending around source/drain regions 34 and adjoining isolation trenches 20, it will be understood that source/drain pockets 32 may extend only along the inside portion of source/drain regions 34 adjoining the channel 24. Alternatively, a deeper source/drain implant may be performed to extend source/drain regions 34 over the bottom portion of source/drain pockets 32. Either one of these well-known methods reduces the capacitance of the transistor, thereby improving transistor performance.

H1

1. A field effect transistor comprising:

a region of semiconductor material doped a first conductivity type;

spaced apart source and drain regions of opposite conductivity type, both said source region and said drain region disposed in said region of semiconductor material and a counterdoped region of first conductivity type disposed within said source region forming a source and within said drain region forming a drain and isolated from the remaining portion of said region of semiconductor material by said source region and said drain region;

a counterdoped channel region disposed in said region of semiconductor material between said source region and said drain region;

said counterdoped channel region having a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region being the primary conduction channel of said transistor and having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source and said drain.

7. A semiconductor device comprising:

#13 J1

a substrate of a first conductivity type containing a plurality of field effect transistors, at least one of the field effect transistors having a counterdoped channel of opposite conductivity type, a source region of said first conductivity type adjacent to the channel, a drain region of said first conductivity type adjacent to the channel and spaced from said source, all disposed in said substrate, and a gate overlying the channel;

said counterdoped channel comprising a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source region and said drain region.

14. A method for forming a field effect transistor, comprising the steps of:

J1 #14

providing a region of semiconductor material doped a first conductivity type;

forming a source region of said first conductivity type and a drain region of said first conductivity type, both said source and said drain disposed in said region of semiconductor material and separated by a counterdoped channel region disposed in said region of semiconductor material;

forming said counterdoped channel region by forming a first region in said channel region of one of undoped or opposite conductivity type;

doping said channel region with a second dopant to form a second doped region underlying the first region of said opposite conductivity type, said second doped region having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source region and said drain region.